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MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



Pruning netlist: a smarter approach to efficient and reliable circuit characterization

Pawan Verma¹, Saurabh Srivastava¹, Anil Kumar Dwivedi¹ Matthieu Fillaud²

¹STMicroelectronics

²Siemens



Motivation

Innovative characterization approach for complex IO designs

Conventional system-level IO interface design:

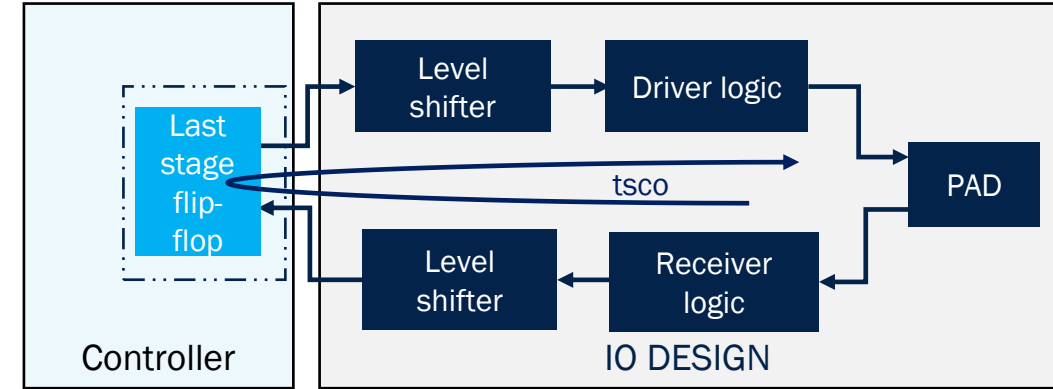
- The controller consists of combinational and sequential logic
- Pure combinational logic is present in periphery IO design

System level IO interface limitations:

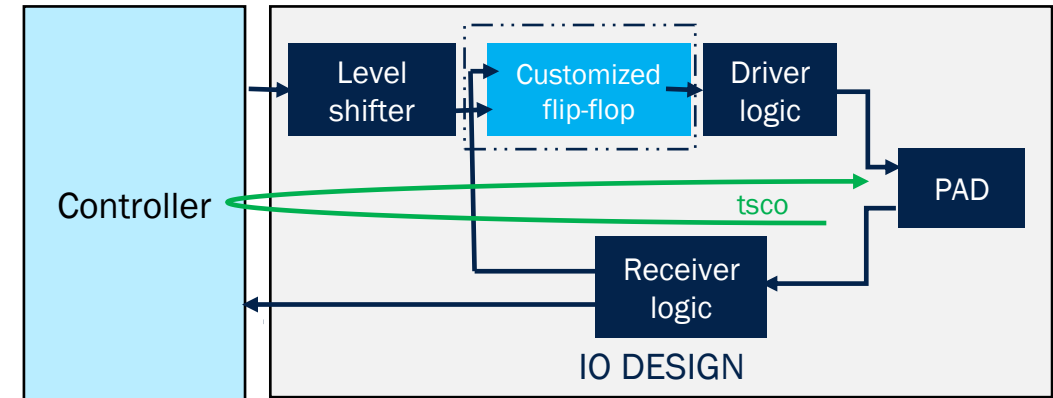
- Clock to data turnaround time (tsco) limits the maximum frequency
- To increase the speed of SoC, tsco need to be minimized

Improved system level IO interface design:

- Last stage flip-flop from controller, placed in periphery IO design
- Customized flip-flop is working on IO voltage level → reduces clock to output delay due to a smaller number of level shifters used



Conventional system-level IO interface design



Improved system level IO interface design

Improved system-level IO block demands for an improvised characterization method to ensure flop timing accuracy

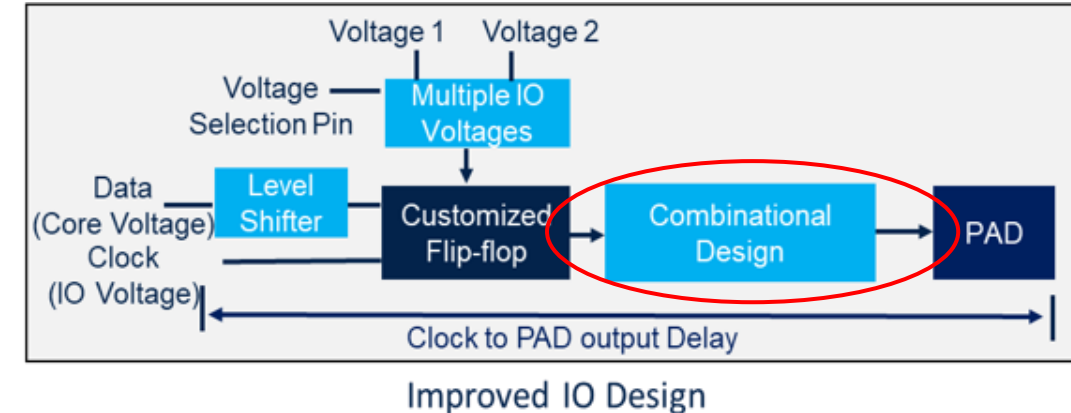
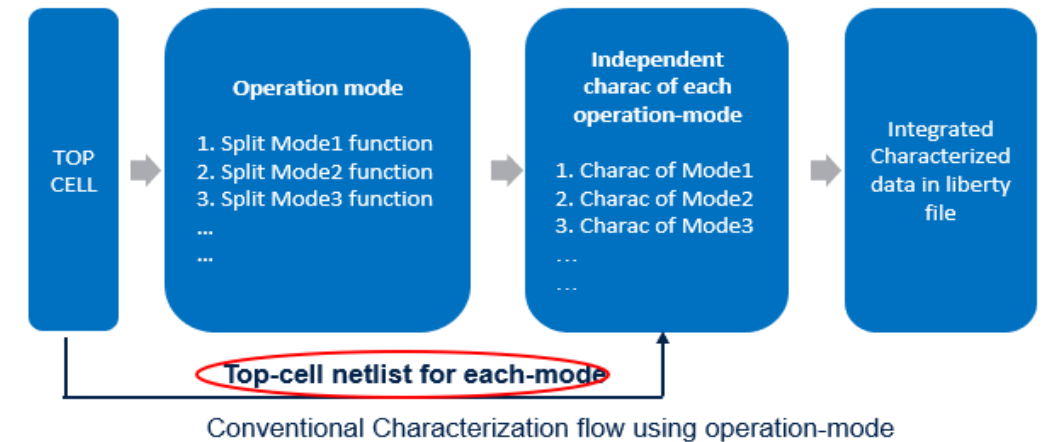
Characterization challenges: Improved system level IO block

Limitations in the conventional characterization method*

- **Longer characterization time**
 - IO designs are complex: multimode, multi-supply
 - Charac tool*: break down top cells into sub cells
 - Parses: full netlist within each sub cell
 - Re-evaluate: all internal nodes, causing longer simulation time
- **Inaccuracy in conventional constraint calculation**

Applying a 10% increase to the already inflated delay value causes inaccurate setup-hold constraint calculation

 - Incorporating combinational design delay into C2Q measurement
 - Inflated C2Q measurement impacts timing analysis



Need a solution that enhances timing precision and simulation efficiency for such complex IO designs

*Kronos: Siemens characterization engine

Proposed solution

Isolate combinational delay and utilize flip flop C-Q for constraint calculation

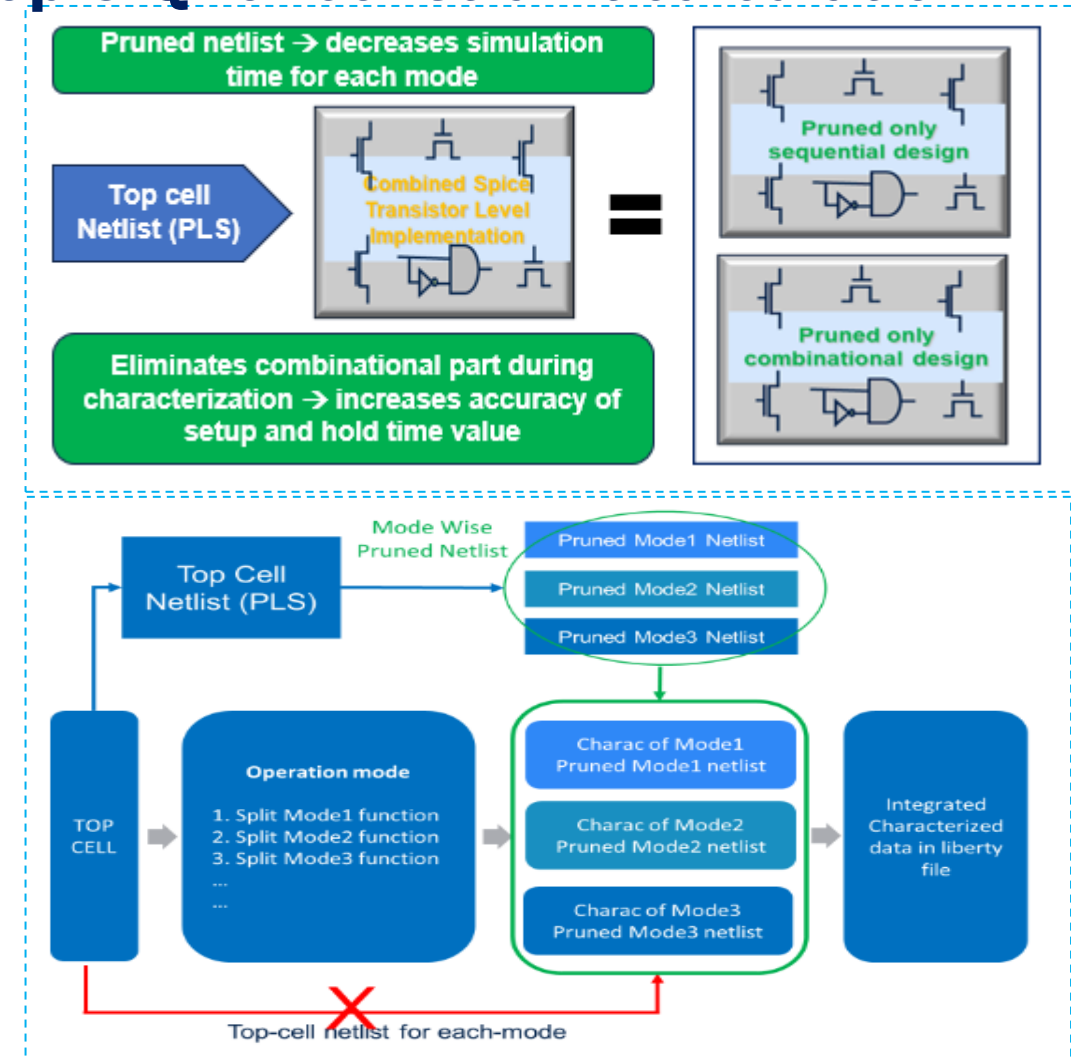
Pruned netlist-based sub cell characterization

- Conventional approach uses a complete top-level netlist for each sub cell
- Proposed pruned-netlist method uses only relevant parts of netlist

Improved characterization time and accuracy

- Significant reduction in characterization time
 - smaller netlist leads to less simulation time for complex circuits
- Closer alignment between simulation and real-world circuit behavior
 - Isolating C2Q delay from PAD delay enhances the precision of setup and hold time measurements

In-house, automated pruning feature developed to demonstrate the methodology



Proposed characterization flow using operation mode

Results

Runtime gain

- Simulation is run on a pruned netlist of only sequential design parts during setup-hold characterization
- Simulator time to evaluate the extra combinational circuit reduced runtime decreased

Cell	Methodology	SPICE simulation time of 1 PVTSC	Total time (50 PVT, 7*7 slope)	Time Gain
Cell1	Conventional	20mn 35s	~50429mn	25.6%
	Proposed	15mn 18s	~37485mn	
Cell2	Conventional	19mn 7s	~46835mn	27.2%
	Proposed	13mn 55s	~34095mn	

Table 1 *PVTSC: process voltage temperature, 1*1 slope load

Constraint timing accuracy

- Setup/Hold, results are more accurate due to the presence of only sequential part during characterization using pruned netlist
- Aligned with the standard characterization methodology of std. cell flip-flop

Constraints	Different slope	Methodology		Diff (%)
		Conventional	Proposed	
Hold time (best case)	SS1	0.3664	0.3987	08.10%
	SS2	0.4594	0.4756	03.40%
	SS3	0.8061	0.8218	01.90%
Setup time (worst case)	SS1	0.1171	0.2431	51.83%
	SS2	0.1953	0.3466	43.65%
	SS3	0.4101	0.5029	18.45%

Table 2 *SS: represents different slope for clock and data pin

Pruned netlist-based characterization is an effective technique to enhance runtime gain and provide more accurate setup hold values due to elimination of combinational part during sequential mode characterization

Summary

Convention design architecture limitation in IO placement & its solution

- Last stage flip-flop from the core is incorporated in the IO ring with combo logic
- Reduces significant clock to data turn around time

Change in design due to conventional design limitations makes IO design complex

- Need to improve characterization time for the complex IO design.
- Accurate characterized value for accurate timing analysis during SoC level

Pruning netlist solution

- Enables faster characterization time (~ 27%) for complex IO designs
- More accurate setup and hold time values (up to 50%) leading accurate timing analysis at the SoC level

Work in progress: Automatic method is in exploration with EDA to generate the pruning netlist for broader adoption and streamlined workflows



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Thank you!

